AMENDMENTS TO THE CLAIMS

Cancel Claims 1-9, 15-17, 26 and 35-37 without prejudice. Please accept amended Claims 10 and 17 as follows.

Listing of claims.

1-9. (Canceled)

10. (Currently Amended) A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors in the integrated circuit, wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second transistors and wherein V_{OUT} is obtained at a common node connection of the first and second transistors, and wherein the DC voltage characteristic data is obtained with the first and second transistor devices operating in a subthreshold region;

determining a distribution of Vt (threshold voltage) mismatch for the selected device pair using corresponding DC voltage characteristic data for the selected device pair;

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; and

characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit,

wherein the step of determining a distribution of Vt mismatch for the selected device pair using the corresponding DC voltage characteristic data for the device pair, comprises the steps of:

determining a distribution of V_{IN} for a given output voltage, V_{OUT}; and

determining a distribution of Vt mismatch of the first and second transistors from the distribution of V_{IN},

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wherein the distribution of V_{IN} corresponds to a distribution of one-half the Vt mismatch between the first and second transistors when the first and second transistors comprise an NFET and PFET.

11. (Original) The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair of an integrated circuit comprises applying a constant gate voltage to a gate of the first transistor and varying V_{IN} applied to a gate of the second transistor such that the first and second transistors of the device pair are maintained in a subthreshold region of operation; and

determining V_{OUT} as a function of the varying V_{IN}.

12. (Original) The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

13. (Original) The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair comprises:

varying V_{IN} applied to gates of the first and second transistors such that the first and second transistors of the device pair are maintained in a subthreshold region of operation; and

determining V_{OUT} as a function of the varying V_{IN}.

14-17. (Canceled)

18. Original) The method of claim 10, wherein the integrated circuit comprises an SRAM (static random access memory) cell.

19. Original) The method of claim 10, wherein the step of determining a Vt variation of transistors in the integrated circuit comprises determining a standard deviation of Vt variation of the transistors.

20-26. (Canceled)

27. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising:

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors in the integrated circuit, wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second transistors and wherein V_{OUT} is obtained at a common node connection of the first and second transistors, and wherein the DC voltage characteristic data is obtained with the first and second transistor devices operating in a subthreshold region;

determining a distribution of Vt (threshold voltage) mismatch for the selected device pair using corresponding DC voltage characteristic data for the selected device pair;

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; and

characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit,

wherein the instructions for determining a distribution of Vt mismatch for the selected device pair using the corresponding DC voltage characteristic data for the device pair, comprise instructions for performing the steps of:

determining a distribution of V_{IN} for a given output voltage, V_{OUT}; and

determining a distribution of Vt mismatch of the first and second transistors from the distribution of V_{IN},

wherein the distribution of V_{IN} corresponds to a distribution of one-half the Vt mismatch between the first and second transistors when the first and second transistors comprise an NFET and PFET.

28. (Canceled)

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29. (Original) The program storage device of claim 27, wherein the distribution of device mismatch comprises a distribution of Vt (threshold voltage) mismatch.

30-31. (Canceled)

32. (Original) The program storage device of claim 27, wherein the instructions for performing the step of obtaining DC voltage characteristic data for a selected device pair comprise instructions for separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

33. (Original) The program storage device of claim 27, wherein the instructions for obtaining DC voltage characteristic data for a selected device pair comprise instructions for performing the steps of:
 varying V_{IN} applied to gates of the first and second transistors such that the first and second transistors of the device pair are maintained in a subthreshold region of operation; and
 determining V_{OUT} as a function of the varying V_{IN}.

34. (Original) The program storage device of claim 27, wherein the instructions for obtaining DC voltage characteristic data for a selected device pair of an integrated circuit comprise instructions for performing the steps of:
 applying a constant gate voltage to a gate of the first transistor and varying V_{IN} applied to a gate of the second transistor such that the first and second transistors of the device pair are maintained in a subthreshold region of operation; and
 determining V_{OUT} as a function of the varying V_{IN}.

35-37. (Canceled)

38. (Original) The program storage device of claim 27, wherein the instructions for determining a Vt variation of transistors in the integrated circuit comprise instructions for determining a standard deviation of Vt variation of the transistors.